Millimeter-wave Resonator Based on High Quality Factor Inductor and Capacitor based on Slow-Wave CPS

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***Abstract*—This work introduces the concept of a quasi-lumped LC resonator integrated in CMOS technology and based on slow-wave transmission lines. The quasi-lumped inductor and capacitor constituting the resonator are synthesized using slow-wave coplanar stripline exhibiting high quality factor and small footprint. The proposed concept is demonstrated at mm-wave frequencies around 40 GHz through the design of a shunt resonator. Good agreement between simulation and measurement is observed.**

***Keywords*—Millimeter-wave, resonator, slow-wave coplanar stripline, high *Q-factor* quasi-lumped components.**

I. Introduction

Due to the increased demand of high data rate wireless communications and high-precision radar systems, the next generation of wireless circuits and systems have been pushed to operate at mm-wave frequencies. As integrated circuits design becomes more challenging at mm-waves and requires more advanced integrated processes, the semi-conductor companies have well accompanied these new trends by proposing new era of CMOS/BiCMOS technologies at the nano-scale. Nonetheless, fewer efforts have been carried out to obtain high quality passive devices, like transmission lines (TLs), capacitors, inductors or transformers as basic passive components. Therefore, during the last decade the poor quality factor (*Q-factor*) of the integrated passive devices was introduced as very critical issue requiring to be addressed. Various topologies have been proposed to realize integrated TLs with high *Q-factor* [1-3]. The most promising among them remain those that use the concept of slow-wave (SW) firstly proposed in [1] for coplanar waveguides (CPW) and in [2] for coplanar striplines (CPS), leading to S-CPW and S-CPS. Models were further developed in [4-5] for S-CPW. The method developed in [5] can also be used to model S-CPS. Next, circuits were designed with the SW concept, mainly based on S-CPW as in [6] where a 60-GHz bandpass filter was realized to demonstrate the performance that could be achieved with S-CPW. The *Q-factor* improvement in SW TLs (S-CPW or S-CPS) is obtained thanks to the use of a shielding layer, which (i) prevents any electric field interaction with the lossy silicon substrate, and (ii) separate magnetic and electric fields (thus slowing the wave). The SW concept also provides the benefit of longitudinal dimensions shrinking, thus leading to shorter TLs; however their width is larger as compared to their µstrip lines counterpart, resulting in comparable areas; the comparison depending on the characteristic impedance that is considered. In [6], resonators were realized by using a distributed approach, e.g. quarter wavelength stubs, thus leading to large footprint, even at mm-waves with SW concept. The size of resonators would be much smaller if lumped components, i.e. lumped capacitors and inductors, were used. However, the *Q-factor* of lumped components in CMOS technologies is quite low. For instance, in [7] authors have reported a measured *Q-factor* of 10 and 15 at 60 GHz for lumped MOM (Metal-Oxyde-Metal) capacitors and lumped spiral inductance, respectively. Of course, the *Q-factor* of lumped inductors and capacitors depends on the stack-up of the used technology as we will demonstrate in the next section. However, *Q-factor* of MOM capacitor decreases with frequency, as shown in [8], where a *Q-factor* lower than 9 was measured at G-band (140-220 GHz) for a MOM capacitor realized in a BiCMOS 55-nm technology from STMicroelectronics while it was around 14 at 60 GHz.

In this paper, the design of an LC resonator based on high-*Q* quasi-lumped components is proposed. Quasi-lumped inductors and capacitors were designed from S-CPSs and used together to fabricate the LC resonator. The S-CPS principle is reminded in section II, where the concept of quasi-lumped inductors and capacitors is also described. Then the parallel LC resonator is designed in section III. Measurement and simulation results are compared, leading to a good agreement, thus validating the proposed concept.

II. Synthesis of High Q-factor Inductor and Capacitor

A. S-CPS presentation

As stated in the introduction the proposed resonator is designed with inductor and capacitor that are realized using the S-CPS structure depicted in Fig. 1. The CMOS 0.35-µm technology of AMS was used. It offers four metal layers, but only two metal layers are necessary for the S-CPS design. The S-CPS is constituted by two strips of width *W* and spacing

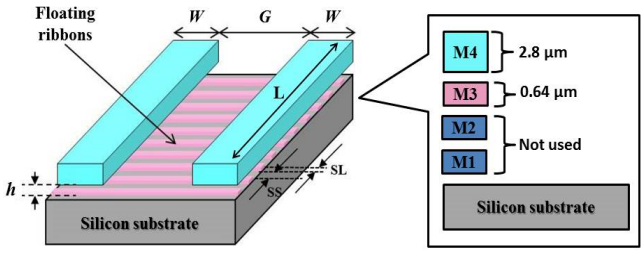


Fig. 1. Structure of the S-CPS in CMOS 0.35-µm AMS process.

G laid out on the top metal layer of the Back-End-Of-Line, and shielded by floating ribbons deposited on a lower metal layer.

From a circuit point of view, the shield brings a capacitive effect, thus increasing the linear capacitance as compared to a classical CPS and leading to slow-wave behaviour. In addition, the presence of the shield cancels the interaction between the electric field and the lossy silicon substrate. Both effects cumulate, thus resulting in *Q-factor* improvement as compared to classical transmission lines such as microstrip, CPS or CPW. As discussed in [4], the floating ribbons constituting the shield must be able to capture the electrical field. Hence their spacing SS must be lower than the height (h) between the CPS strips and the floating ribbons. Also, their width must be limited to avoid eddy current losses, but not too narrow to limit the metallic losses. To meet these requirements, SL and SS were set to $0.6\ \mu m$ and $1\ \mu m$, respectively, for all the designs presented hereinafter.

B. Inductor design

Going from the S-CPS as basic block, a high *Q-factor* inductor can be synthesized. In this section it will be shown that the input impedance of a shorted S-CPS can be equivalent to a lumped inductor. Let's consider the equivalence shown in Fig. 2; the input impedance calculated using *ABCD* matrix for a lossless S-CPS is expressed in (1).

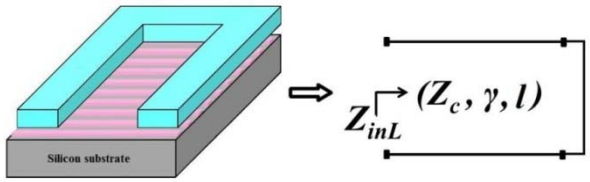


Fig. 2. Equivalent model for shorted S-CPS.

$$Z_{in_L} = \frac{B}{D} = Z_C \cdot tanh(\beta \cdot l) \qquad (1)$$

where Z_C is the S-CPS characteristic impedance, and β its propagation constant, respectively.

Therefore, the shorted S-CPS behaves like inductor owning an equivalent inductance formulated as follows:

$$L_{eq} = Z_C \cdot tan(\beta \cdot l)/\omega \qquad (2)$$

The synthesis of a given value of inductance to fulfill particular design needs is done by varying the parameters of the shorted S-CPS, namely, the strips' width (W), the gap (G), the length (L) and the height (h). Fig. 3 illustrates charts drawn at 40 GHz showing how the *Q-factor* and inductor value can be controlled according to the S-CPS parameters. Of course, losses were taken into account to extract the *Q-factor*. The metal thicknesses and conductivity were fixed to $2.8\ \mu m$ and $30 \cdot 10^6\ S/m$, respectively. The S-CPS overall width $D = W + 2G$ was fixed to $50\ \mu m$, i.e. when G increases, W decreases. A higher value of D would lead to higher performance, but also larger area. It can be noted from Fig. 3(a) that the increase of (L) leads to higher inductance and lower *Q-factor*. The *Q-factor* decreases with L since the distributed behavior of the S-CPS is getting stronger. The *Q-factor* reaches a maximum for $G = 20\ \mu m$ $(W = 15\ \mu m)$; when (G) increases, the magnetic flux increases, thus leading to an increase of the inductance value, but (W) decreases, thus leading to higher metallic losses. A tradeoff seems to appear around $G = 20\ \mu m$. From Fig. 3(b), it is seen that the higher the (h), the higher the *Q-factor*. For instance, $h = 2.5\ \mu m$, (means that the shield is laid out on lower metal layer) leads to higher *Q-factor* in comparison with the case when $h = 0.5\ \mu m$ (the shield is deposited on higher metal layer). However, in the latter case, more slow-wave effect is crated, thus leading to smaller longitudinal size of the inductor. Therefore, by managing the four design parameters offered by this structure $(h,\ G, L$ and $W)$, a tradeoff should be made between the foreseen inductance value, its *Q-factor* and its size.

Fig. 4 aims to figure out the advantage of the S-CPS inductor against two configurations of conventional lumped spiral inductor i.e. symmetric and differential.

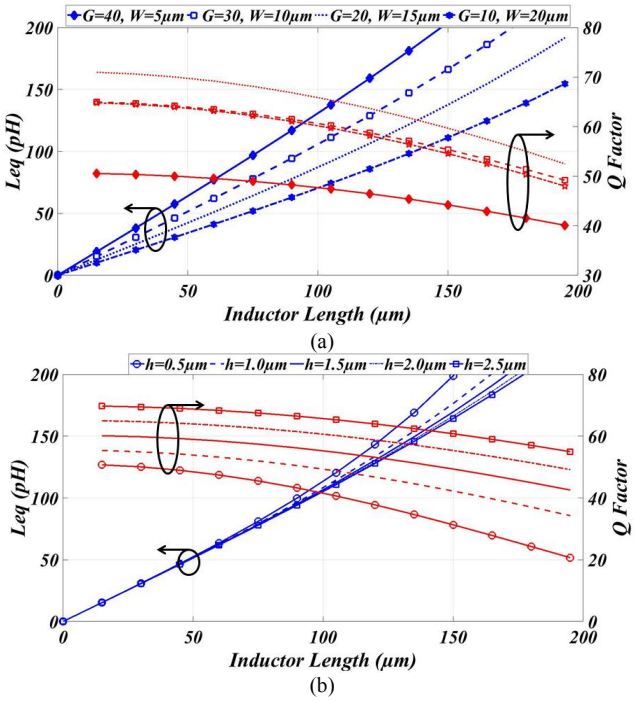
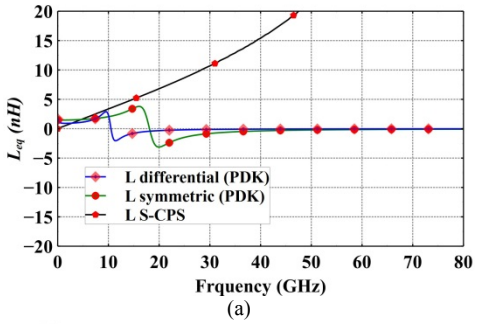
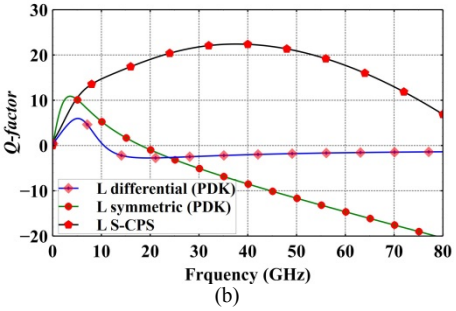


Fig. 3. Variation of the inductance and *Q-factor* of the S-CPS inductor as function of geometric parameters at 40 GHz.

To fairly compare, the three inductors were implemented in the same CMOS process (CMOS $0.35\ \mu m$ of AMS) and for the same inductance value of 1 nH. This value was chosen because it is the smallest synthesizable one in the mentioned technology. From Fig. 4 (a) it can be seen that the conventional inductors available in the technology cannot be used at mm-waves due to the very low self-resonance frequency (SRF), whereas the resonance of the S-CPS inductor occurs at 90 GHz. In addition, Fig. 4 (b) illustrates how the *Q-factor* of the S-CPS inductor is clearly higher over



(a)



(b)

Fig. 4. Comparison of the S-CPS inductor and conventional spiral inductor included in the CMOS 0.35 µm AMS PDK, up to 80 GHz. (a) Inductance value (b) *Q-factor*.

a wide frequency range. Moreover, the size of the S-CPS inductor is smaller, with a surface equal to $100x150\ \mu m^2$ against $472x452\ \mu m^2$ and $351x353\ \mu m^2$ for symmetric and differential spiral inductors, respectively. Another very important aspect of the S-CPS inductor is the design flexibility: various geometrical dimensions can be chosen to reach a particular performance. This is highly appreciated when an advanced technology is used where the technological constraints are stronger.

C. Capacitor design

This sub-section describes how the S-CPS can be used in order to design very high *Q-factor* integrated capacitor. In this case, let's compute the impedance seen from one end of S-CPS while its second end is left open (the two strips are not connected). The input impedance is expressed as (4):

$$Z_{in_{cap}} = \frac{A}{C} = Z_C/tanh(\gamma \cdot l) \quad (4)$$

By considering lossless TL the equivalent capacitor can be deduced from (4) as follows:

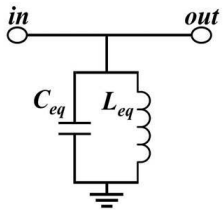
$$C_{eq} = \frac{tan(\beta \cdot l)}{\omega \cdot Z_C} \quad (5)$$

Obviously any given value of capacitance can be obtained by varying the geometric parameters of the open circuited S-CPS, in the same way as for the inductor.

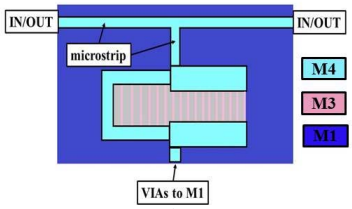
III. Resonator Design and Measurement

As a proof of concept based on the inductor and capacitor proposed in the previous section, the LC resonator depicted in Fig. 5(a) was designed and implemented in the 0.35-µm CMOS process from AMS. Its layout is depicted in Fig. 5(b) while the photography of the fabricated chip is presented in Fig. 6. The S-CPS inductor and capacitor are connected in parallel and fed over a microstrip line T-junction. The stack-up of the microstrip line is M4 layer for signal strip and M1 layer for ground. The S-CPS based inductor and capacitor were designed using the stack-up illustrated in Fig. 1, i.e. the strips were laid out on M4 and the shield on M3, respectively. In order to reproduce the ideal schematic of Fig. 5, one of the S-CPS strips is connected to ground (M1) through a set of vias to control the return-current path and hence the electric field distribution. Therefore, the two S-CPSs behave well as quasi-lumped inductor and quasi-lumped capacitor as predicted by the theoretical study presented in previous section. The final retained geometric dimensions and their equivalent lumped behaviour are showed in Table 1. As can be seen, the reached *Q-factor* at 40 GHz for the designed capacitor and inductor are 27 and 22, respectively. Such values could not be obtained with the lumped components provided in the PDKs associated to the used technology.

Aiming to understand the principle behind the proposed resonator, the equivalent-circuit models in Fig. 7 are proposed. Indeed, the excitation of the resonator is performed through T-junction of 50-Ω microstrip lines, the vias were modelled by a resistor in series with an inductance and the return-current path was accounted in this latter; these three parameters were quantified using the quasi-static extractor Maxwell 3D. The distributed model introduced in [9] was utilized for the S-CPS in Fig. 7(b), the S-CPS being modelled by n sections of LRCR electrical circuit. Each section is associated to S-CPS length of $SS/2 + SL + SS/2$, which corresponds to one ribbon with length (SL) trapped between two half-gaps ($SS/2$).



(a)



(b)

Fig. 5. LC shunt parallel resonator (a) ideal electrical schematic. (b) Layout.

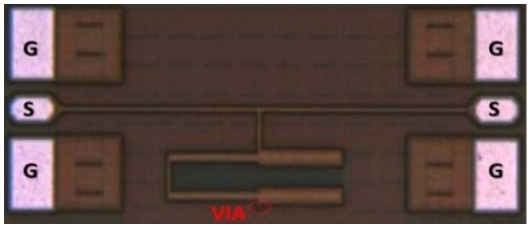


Fig. 6. The chip photo of the fabricated resonator.

Table 1. Parameters of S-CPS Inductor and Capacitor.

	W (µm)	G (µm)	L (µm)	h (µm)	L_{eq} (pH)	C_{eq} (fF)	*Q-factor*
S-CPS inductor	10	40	134	1	154	-	22
S-CPS capacitor	20	30	132	1	-	53	27

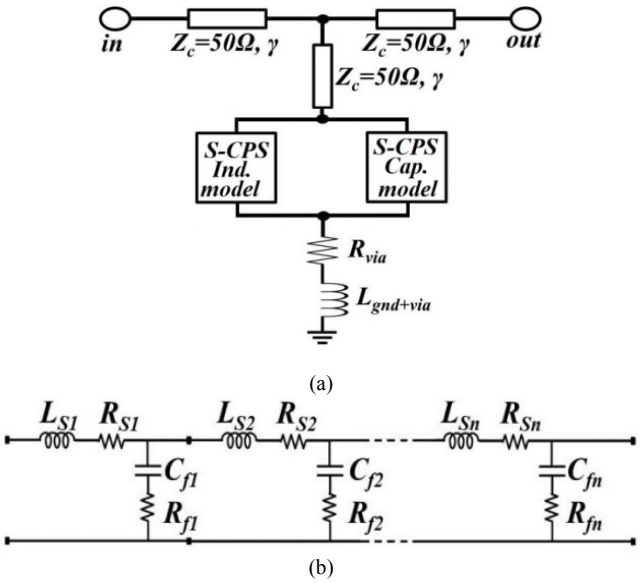


Fig. 7. Electrical model. (a) The proposed resonator. (b) S-CPS model

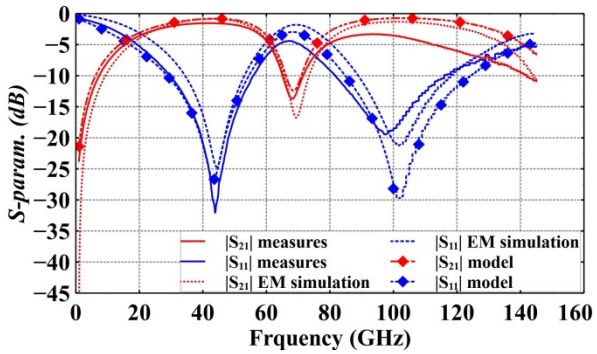


Fig. 8. Resonator response.

The measured S-parameters of the proposed resonator are showed in Fig. 8 versus the 3D EM simulations using ANSYS HFSS as well as the response of the electrical circuit model. The characterization was performed using an Anritsu VectorStar® ME7838A4 VNA from 70 kHz to 145 GHz. An on-wafer TRL calibration was carried out. As observed, good agreement was achieved, since the resonance occurs at 44 GHz for the three plots, in addition, the shapes of the EM simulation and the measurement are quasi-similar. The measured mid-band insertion loss is 1.5 dB against 0.85 dB for the EM simulation. The measured return loss is better than 30 dB. Moreover, the model is in good agreement with both the EM simulation and the measurement.

IV. Conclusion

The design of a mm-wave resonator around 40 GHz was presented. It was designed based on an original configuration of high quality factor inductor and capacitor. These two components were synthesized thanks to the features provided by the slow-wave coplanar stripline. The implementation on 0.35-µm CMOS process of AMS has shown very good agreement between measurement, EM simulation and the deemed electrical model. The proposed resonator can be considered as a promising device to be considered in IC mm-wave designs. Even if the AMS 0.35-µm technology is not dedicated to mm-wave designs, the work reported in this paper could be easily done on more advanced technology. The authors selected this technology for a proof-of-concept due to its low price.

References

[1] T. S. D. Cheung, J. R. Long, K. Vaed, R. Volant, A. Chinthakindi, C. M. Schnabel, J. Florkey, and K. Stein, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2003, pp. 396–397.

[2] M. Abdel Aziz, H. Issa, D. Kaddour, F. Podevin, A.M.E. Safwat, E. Pistono, J.-M. Duchamp, A. Vilcot, J.-M. Fournier, and P. Ferrari, "Slow-wave high-Q coplanar striplines in CMOS technology and their RLCG model," *Microwave and Optical Technology Letters*, vol. 54, no. 3, pp. 650-654, March 2012.

[3] Y. Belaroussi, M. Rack, A.A. Saadi, G. Scheen, M.T. Belaroussi, M. Trabelsi, and J.-P. Raskin, "High quality silicon-based substrates for microwave and millimeter wave passive circuits," *Journal of Solid-State Electronics*, vol. 135, pp. 78-84, June 2017.

[4] A.-L. Franc, E. Pistono, G. Meunier, D. Gloria, and P. Ferrari, "A Lossy Circuit Model Based on Physical Interpretation for Integrated Shielded Slow-wave CMOS Coplanar Waveguide Structures," *IEEE Trans. on Microwave Theory Tech.*, vol. 61, no. 2, pp. 754-763, Feb. 2013.

[5] A. Bautista, A.-L. Franc, and P. Ferrari, "Accurate Parametric Electrical Model for Slow-Wave CPW and Application to Circuits Design," *IEEE Trans. on Microwave Theory Tech.*, vol. 63, no. 12, pp. 4225 - 4235, Dec. 2015.

[6] A.-L. Franc, E. Pistono, D. Gloria, and P. Ferrari, "High-performance Shielded Coplanar Waveguides for the Design of CMOS 60-GHz Band-pass Filters," *IEEE Trans. on Electron Device*, vol. 59, no.5, pp. 1219 - 1226, May 2012.

[7] J. Shi, K. Kang, Y. Z. Xiong, J. Brinkhoff, F. Lin and X. Yuan, "Millimeter-Wave Passives in 45-nm Digital CMOS," *IEEE Electron Device Letters*, vol. 31, no. 10, pp. 1080-1082, Oct. 2010.

[8] A.A. Saadi, M. Margalef, S. Le Pilliet, C. Gaquière, D. Gloria, C. Durand and P. Ferrari," MOM Capacitance Characterization in G-Band using On-wafer 3D-TRL Calibration," *in Proc. 49th European Microwave Conference (EuMC)*, 28 Sept. – 4 Oct., 2019, Paris, France.

[9] A. Bautista, M. A. Aziz, F. Podevin and P. Ferrari, "A predictive model for Slow-wave Coplanar Striplines in integrated technologies," *IEEE MTT-S International Microwave Symposium* (IMS), May 17-22, 2016, San Francisco, CA, USA.